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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,308	01/23/2004	Shreesh Narasimha	FIS920020200US2 (16106A)	6529

23389 7590 06/25/2004

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
GARDEN CITY, NY 11530

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,308	NARASIMHA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01/23/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 18 is objected to because of the following informalities: There is no antecedent basis for the claimed limitation "said silicide region" as claimed in claim 18. Appropriate correction is required. The examiner suggests "said first silicide region".

Claim 19 is objected to because of the following informalities: There is no antecedent basis for the claimed limitation "said silicide region" as claimed in claim 18. Appropriate correction is required. The examiner suggests "said first silicide region".

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5, 10-12, 15, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,063,681 to Son.

Regarding claim 1, Son (figures 3A-H) teaches a method for forming a low resistance MOSFET device comprising the steps of:

forming a gate region (25) atop a surface of substrate (21);

forming first spacers (26) having a first spacer width on sidewalls of the gate region (25);

forming first silicide regions (29) having a first silicide thickness (100 – 200 Angstroms) in the substrate (21) as well as atop a surface of the gate region (25);

forming second spacers (31) having a second width greater than the first spacer (26) width (figure 3H) on the substrate (21), wherein the second spacers (31) protect the first silicide region (29) in the substrate (21); and

forming second silicide regions (33) in the substrate (21) and atop a surface of the gate region (25), wherein the second silicide regions (33; 100 – 300 Angstroms) have a thickness that is greater than the first silicide thickness (29; 100 – 200 Angstroms).

Regarding claim 5, Son teaches forming source/drain extension regions (27) following the gate region formation.

Regarding claim 10, Son teaches forming deep source/drain regions (30) after forming the first spacers (26).

Regarding claim 11, Son teaches forming the deep source/drain regions (30) comprises ion implantation of N-type (column 3, lines 64-66). Therefore, it inherently teaches the deep source/drain regions (30) comprise ion implantation of Arsenic or Phosphorous (a type V element) into the substrate (21).

Regarding claim 12, Son teaches forming of the first silicide region (29) comprises depositing a first metal layer (28) upon an exposed surface of the substrate (21) and annealing (column 3, lines 58-62).

Regarding claim 15, Son teaches the thickness of the first silicide region (29) is 100 – 200 Angstroms (10 – 20 nm), which is in the range (1 – 20 nm) of the claimed invention.

Regarding claim 16, Son teaches the thickness of the first silicide region (29) is 100 – 200 Angstroms (10 – 20 nm), which is in the range (2 – 15 nm) of the claimed invention.

Regarding Claim 17, Son teaches the thickness of the first silicide region (29) is 100 – 200 Angstroms (10 – 20 nm), which is in the range (5 –12 nm) of the claimed invention.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,063,681 to Son in view of US Patent No. 6,313,020 to Kim et al.

Regarding claim 2, Son differs from the claimed invention by not showing the forming of the gate region further comprises predoping of the gate region. However, Kim et al. teach forming of the gate region comprising predoping process (column 1, lines 26-34). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kim et al. into the device taught by Son because it improves the depletion of electrons of the gate electrode.

Regarding claim 3, the combined device shows the predoping is preformed by ion implantation of a type III-A element (Kim et al.; Boron; lines 30-34).

Regarding claim 4, the combined device differs from the claimed invention by not showing predoping is achieved via ion implantation of phosphorus into the gate region.

Phosphorous and arsenic are known donors. It would have been obvious to select known donor atoms since they are well suited for the intended use.

5. Claims 6-9, 13, 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,063,681 to Son.

Regarding claim 6, Son differs from the claimed invention by not showing the first spacer width is from about 5nm to about 20 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first spacer width is from about 5nm to about 20 nm because it protects the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 7, Son differs from the claimed invention by not showing the first spacer width is from about 7 nm to about 15 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first spacer width is from about 7 nm to about 15 nm because it protects the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 8, Son differs from the claimed invention by not showing the second spacers width is from about 20 nm to about 90 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the second spacers width is from about 20 nm to about 90 nm because it protects the gate electrode. Furthermore, it has been held

that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 9, Son differs from the claimed invention by not showing the second spacers width is from about 30 nm to about 70 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the second spacers width is from about 30 nm to about 70 nm because it protects the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 13, Son differs from the claimed invention by not showing the first metal layer has a thickness from about 2 nm to about 7 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first metal layer has a thickness from about 2 nm to about 7 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Son teaches the first metal layer comprises Ta (column 4, lines 5-6).

Regarding claim 18, Son teaches the first silicide region (29) is formed in the substrate (21) having a channel region (a portion of region is located under the gate and between the source/drain extension regions [27]) beneath the gate region.

Son differs from the claimed invention by not showing the distance between the first silicide region and the channel region is from about 2 nm to about 15 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the distance between the first silicide region and the channel region is from about 2 nm to about 15 nm, since

it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 19, Son teaches the first silicide region (29) is formed in the substrate (21) having a channel region (a portion of region is located under the gate and between the source/drain extension regions [27]) beneath the gate region.

Son differs from the claimed invention by not showing the distance between the first silicide region and the channel region is form about 3 nm to about 10 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the distance between the first silicide region and the channel region is form about 3 nm to about 10 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
June 21, 2004

Donghee Kang
Primary Examiner
A.U. 2811